Energy Consumption Behavior of Modern SSD and Its Architectural Implication

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Abstract

It is hard to identify the internal information of SSD FTL because it is proprietary of manufacturer and it is not subjected to the public. SSD is walking similar path as HDD; core technology of SSD is not open to the public too. However, research community has toiled to identify the internal information of HDD and found ways to describe its details. The problem is that the technique applied for HDD is not adequate for SSD because HDD exploits mechanical movements to locate the data; SSD finds it by measuring the charges in a flash memory cell. In this paper, we present power consumption analyzing technique that allows identifying the mapping algorithm of SSD especially how parallelism is implemented in SSD. All write request and program to flash memory in SSD is divided into channels and ways. Proposed technique allows understanding of when channels and ways are activated.

Proposed method is based on power consumption measurements. Two key concepts in power consumption analysis are channel and way. Channel is technique incorporated in SSD to maximize internal parallelism in SSD. Channel is group of packages of flash chips. Channel technique can reduce program time by dividing a write request to the number of channel. Number of assigned channel in FTL is denoted as N_C and write time with one channel is denoted as T_C. Mathematical derivation for program time is T_C/N_C. Number of channels used in a single write request changes power consumption. Write power consumption with one channel is denoted as P_C. Increment in power consumption can be measured as P_C/N_C. Number of active channels is accounted by measuring power consumption of each write requests and locating range where power consumption varies. Second concept is Way. It is another strategy exploited in SSD to maximize the speed. Difference of way compared to channel is that way affects chips in a package which in general exploits 3D stacking technology. Total number of way is total number of flash-memory connected to one channel. A write request is first divided into sub-write requests and sent over to channels with time-interleaving scheme, and then sub-write requests are programmed in flash memory cells. Number of active ways are denoted as N_W and active time of a way is denoted as T_W. Peak power consumption of active number channels shows no variation, however it shows that range of total duration of power consumption is increased by T_W/N_W. Number of active ways is accounted by measuring power consumption of each write requests and locating duration of power consumption.

We verify how channels and ways operate through experiment. Target device is Intel X-25M. Intel X-25M has 10 channel with 4KB page size and 20 flash-memory packages. We assume that when a write request is less than page size, then FTL does not activate channel or way, and 4KB write request activate only 1 channel and 1 way. Figure 1 shows how channel and way operate when write request size is incremented with factor of two. It shows that write request of 4KB and 8KB have same power consumption with same duration. This shows that 8KB write request activates single channel and single way. Similarly all write requests are measured. 512KB write request exploits 10 channels. Two channels has 16 way active and the rest has 12 ways active. 16 way used in 512KB write defines peak power consumption.

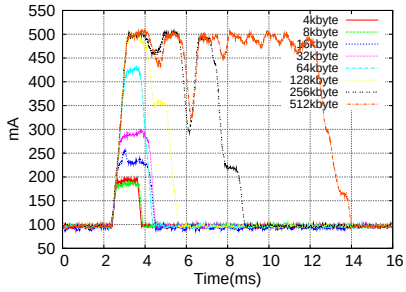

Figure 1: Intel X-25M Total Power Consumption

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